Electronic Version
Stylesheet Version v1.1.1

Description

KEYBOARD

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a keyboard, and more specifically, to a keyboard wherein a processor reads input data only when a key cell is pressed or released.

[0003] 2. Description of the Prior Art

[0004] Please refer to Fig.1 showing a block diagram of a conventional keyboard 10. The keyboard 10 includes a matrix key module 12 and a processor 14 electrically connected to the matrix key module 12. The matrix key module 12 includes a plurality of key cells arranged in matrix, and the processor 14 reads input signals on output ends B_0 to B_7 of the key cells within the matrix key module 12 by polling.

[0005] It is a disadvantage of the prior art that, whenever any key cell within the matrix key module 12 is pressed, the processor 14 needs to continuouslypoll the input signals on

the output ends B_0 to B_7 of the key cells until every key cell within the matrix key module 12 is released. This continuous polling lowers the efficiency of the processor 14.

SUMMARY OF INVENTION

[0006] It is therefore a primary objective of the present invention to provide a keyboard wherein a processor reads input signals on an output end of a key cell within a key module only when any of the key cells within the key module are pressed or released.

[0007] Briefly summarized, a keyboard includes a key module comprising at least one key cell with an output end selectively connected to a first voltage or a second voltage, a detect circuit electrically connected to the output end of the key cell for generating a control signal whenever the voltage on the output end of the key cell becomes the second voltage or the first voltage, a parallel-to-serial register electrically connected to the output end of the key module, and a processor electrically connected to the parallel-to-serial register and the detect circuit for controlling the parallel-to-serial register according to the control signal. The processor controls the parallel-to-serial register to first do a parallel read of the input signals on the

output end of the key cell,and then serially reads the input data input from the parallel-to-serial register.

[0008] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0009] Fig.1 is a block diagram of a conventional keyboard.

[0010] Fig.2 is a block diagram of a keyboard according to the present invention.

[0011] Fig.3 is a waveform diagram of the transient voltage and the control signal detected by the detect circuit whenever the key cells are pressed or released.

Detailed Description

[0012] The keyboard according to the present invention controls a processor, which inputs signals from the key cells within a key module through a parallel-to-serial register. The processor inputs the key signals according to a control signal generated when a voltage in a capacitor changes, which occurs at the moment a detect circuit detectsthat a key cell within the key module has been pressed or re-

leased.

[0013] Please refer to Fig.2 showing a block diagram of a keyboard 50 according to the present invention. The keyboard 50 includes a key module 52 which has at least one key cell (for example, key cells 60, 61 in Fig.2), a detect circuit 54 electrically connected to output ends OUT_{60}, OUT_{61} of the key cells 60, 61 within the key module 52, and a parallel-to-serial register 56 electrically connected to output ends OUT_{60}, OUT_{61} of the key cells 60, 61.A processor 58 is electrically connected to the parallel-to-serial register 56 and the detect circuit 54 for controlling the parallel-to-serial register 56 to read input data from the output ends OUT_{60}, OUT_{61} of the key cells 60, 61 according to a control signal CS from the detect circuit 54.

[0014] The key cells 60, 61 within the key module 52 include switches SW_{60}, SW_{61} respectively. The output end OUT_{60} of the key cell 60 (as well as the output end OUT_{61} of the key cell 61) is electrically connected to either a first voltage Vcc or a second voltage GND according to the opening and closing of the switch SW_{60}. That is, when the key cell 60 is pressed, the switch SW_{60} is turned off and the output end OUT_{60} is electrically connected to the second voltage GND so that a logic low voltage V_L is output. On

the contrary, when the key cell 60 is released, the switch SW_{60} is turned on and the output end OUT_{60} is electrically connected to the first voltage Vcc so that a logic high voltage V_H is output. The logic high signal and the logic low signal on the output ends $OUT_{60,}$ OUT_{61} form the input signals to the parallel-to-serial register 56.

[0015] The detect circuit 54 includes one capacitor corresponding to each key cell within the key module 52 (as shown by capacitors 64, 65 corresponding to the key cells 60, 61 respectively within the key module 52 in Fig.2).An amplifier 66 is electrically connected to the capacitors 64, 65 for amplifying the voltage in the capacitors 64, 65.Two comparators 68, 70 areelectrically connected to the amplifier 66 for comparing the voltage output by the amplifier 66 and outputting the control signal when the voltage output from the output end OUT_{amp} of the amplifier 66 is in a predetermined range.Finally, an OR gate is electrically connected to the comparator 68, 70.

[0016] At the moment when the key cell 60 (similar for key cell 61 or any other key cell) within the key module 52 is pressed or released, the switch SW_{60} of the key cell 60 is accordingly switched off or switched on, and the output end OUT_{60} is accordingly electrically connected to the sec-

ond voltage GND or the first voltage Vcc. In this situation, the detect circuit 54 detects a transient voltage V_{ts} of 100-150mV formed in the capacitor 64 (or the capacitor 65). Please refer to Fig.3 showing a waveform diagram of the transient voltage V_{ts} and the control signal CS in the capacitors 64, 65 detected by the detect circuit 54 whenever the key cells 60, 61 within the key module 52 of the key board 50 are pressed or released. As shown in Fig.3, at the moment when the key cell 60 (similar for key cell 61) is pressed at time t_1 (or t_2), the switch SW_{60} of the key cell 60 is switched off, and the output end OUT_{60} of the key cell 60 is connected to the second voltage GND (i.e. the input signal on the output end OUT_{60} of the key cell 60 becomesa logic low voltage V_L). In this situation, the detect circuit 54 detects a negative transient voltage V_{ts-} in the capacitor 64. On the hand, at the moment when the key cell 60 (similar for key cell 61) is pressed at time t_3 (or t_4), the switch SW_{60} of the key cell 60 is switched on, and the output end OUT_{60} of the key cell 60 is connected to the first voltage Vcc (i.e. the input signal on the output end OUT_{60} of the key cell 60 becomes a logic high voltage V_H). In this situation, the detect circuit 54 detects a positive transient voltage V_{ts+} in the capacitor 64. The ampli-

fier 66 amplifies the positive transient voltage V_{ts+} and the negative transient voltage V_{ts-} and outputsthe amplified positive transient voltage V_{ts++} and the amplified negative transient voltage V_{ts--} into an input end of the comparators 68, 70. In the present invention, the comparators 68, 70 are divided into a positive comparator 68 and a negative comparator 70.The detect circuit 54 outputs the control signal CS from an output end OUT_{or} of the OR gate 72 when either the amplified positive transient voltage V_{ts++} exceeds a positive reference voltage V_{ref+} on the other input end of the positive comparator 68, or when the amplified negative transient voltage V_{ts--} is lower than a negative reference voltage V_{ref-} on the other input end of the negative comparator 70.

[0017] After receiving the control signal CS, the processor 58 controls the parallel-to-serial register 56 to first do a parallelinput of the output ends of all the key cells within the key module 52, and then gradually inputs the input signals serially. For example, when receiving the control signal CS at time t_1, the processor 58 controls the parallel-to-serial register 56 to firstdo a parallel input ofthe input data (01) on the output ends OUT_{60}, OUT_{61} of all of the key cells 60, 61, and then gradually inputs the input

signal (01) serially. As another example, at times t_2,t_3, and t_4, the processor 58 controls the parallel-to-serial register 56 to first do a parallel input of the input data (00), (10), (11), and then gradually reads the input signals (00), (10), (11) serially. The processor 58 can execute specific operations according to these input signals or a variation of the input signals, which is the same as the prior art, so that a further description is hereby omitted.

[0018] In contrast to the prior art, the keyboard according to the present invention includes a key module, a detect circuit, a parallel-to-serial register and a processor. The detect circuit detects the variation between current input signals and previous input signals input by the key module, that is, the detect circuit detects whether any of the key cells within the key module is pressed or released. The processor inputs the current input signals only when the input signals change. Therefore, the keyboard according to the present invention solves the problem of the prior art that continuous polling is required whenever any key cell is pressed (e.g. from time t_1 to t_4 in Fig.3), and thereby improves the efficiency of the processor.

[0019] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made

while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.